Product Brief

OVERVIEW

The EV10AS940 is a 10-bit Ka-band capable single channel Analog-to-Digital Converter (ADC) allowing a sampling rate up to 12.8GSps. It features Digital Down Conversion (DDC) and Fast Frequency Hopping (FFH) capabilities with multiple digital channels thanks to the integration of multiple NCOs. The EV10AS940 is packaged with an organic substrate to allow high speed and high bandwidth operations.

FEATURES

- -3dB Analog Bandwidth: 35.5GHz
- Up to 12.8GSps Conversion Rate
- Single-Ended RF and clock inputs with on-chip DC block and 50Ω adaptation
- On chip calibration
- 10-bit resolution
- 500mVpp full scale input dynamic range
- Digital Down Conversion (DDC)
  - 4 DDC channels, with 4 NCOs per channel
- Fast Frequency Hopping, with deterministic controls and 3 hop options:
  - RTZ
  - Phase Continuous
  - Coherent on 4 frequencies
- Digital Fractional delay for Beam Forming applications
- 11 synchronous HSSL
- ESIstream 62/64b protocol
- 3.3V / 1.8V / 1.2V / 0.9V power supply
- Flexible 1.2V to 1.8V SPI supply
- Power consumption: 2.5W
- 16.0x17.6mm² organic FCBGA
- 350 balls (SAC305) with 0.8mm pitch
- RoHS (Pb-Free)
- Space Grade

PERFORMANCE

- ENOB: 7.0 bits
- Fs=6.6GHz, Fin=14.1GHz, Pout=-6dBFS
  - SFDR = -52dBc
  - H2 = -61.8dBc / H3 = -52dBc
- Fs=6.6GHz, Fin=17.4GHz, Pout=-6dBFS
  - SFDR = -54.1dBc
  - H2 = -54.1dBc / H3 = -55.1dBc
- Fs=10.3GHz, Fin=28.4GHz, Pout=-6dBFS
  - SFDR = -47.5dBc
  - H2 = -47.5dBc / H3 = -50.2dBc
- Fs=12.8GHz, Fin=4.1GHz, Pout=-6dBFS
  - SFDR = -54.5dBc
  - H2 = -61dBc / H3 = -54.6dBc
- Fs=12.8GHz, Fin=14.1GHz, Pout=-6dBFS
  - SFDR = -50.2dBc
  - H2 = -58.5dBc / H3 = -50.2dBc
- Fs=12.8GHz, Fin=17.4GHz, Pout=-6dBFS
  - SFDR = -50.4dBc
  - H2 = -59.8dBc / H3 = -50.4dBc
- Fs=12.8GHz, Fin=28.4GHz, Pout=-6dBFS
  - SFDR = -50.5dBc
  - H2 = -50.5dBc / H3 = -54dBc
- Fs=12.8GHz, Fin=40.5GHz, Pout=-6dBFS
  - SFDR = -32.1dBc
  - H2 = -32.1dBc / H3 = -43.4dBc

APPLICATION

- SatCom
- SAR
- 5G
- P2P communications

Table of Content

1. DOCUMENT HISTORY

Issue	Date	Comments
A	November 2022	Document creation

2. BLOCK DIAGRAMS

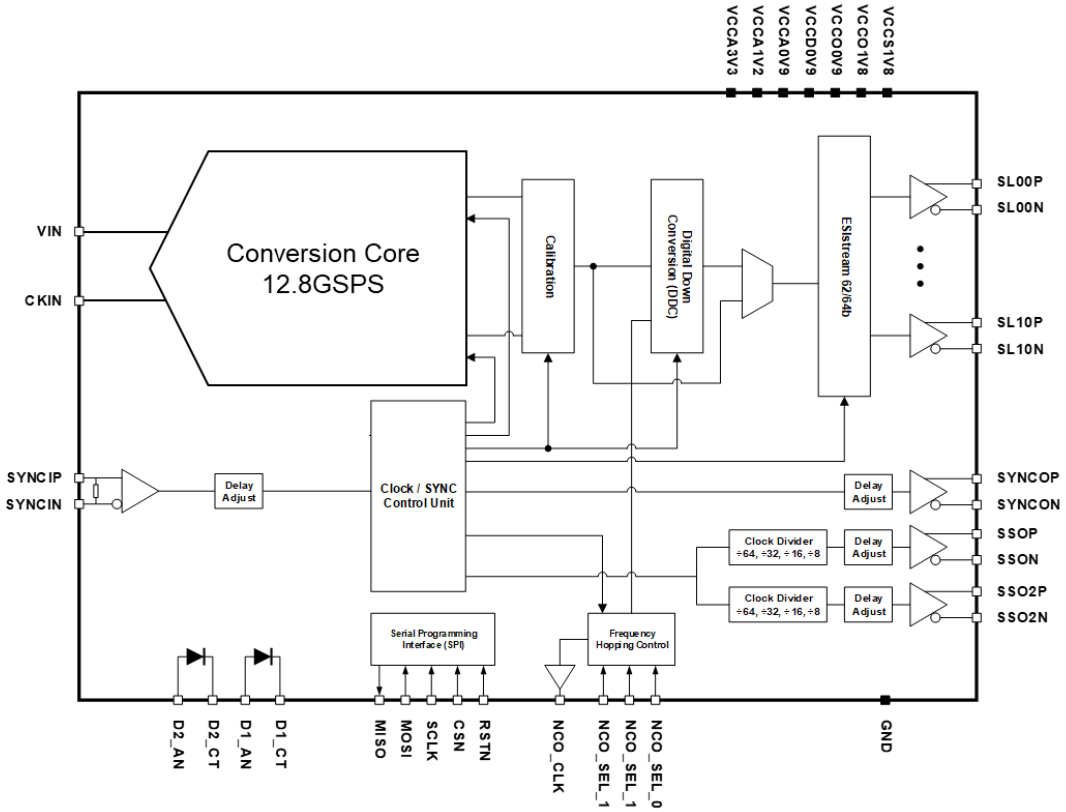

Figure 1 : EV10AS940 Block Diagram.

3. DESCRIPTION

EV10AS940 is a high-performance single channel, 10-bit, 12.8GSps Analog-to-Digital Converter (ADC) that allows sampling of RF signals up to the Ka-band. The high analog input bandwidth (34GHz) makes the EV10AS940 an excellent candidate to address RF direct conversion architectures up to Ka-Band.

The device operates with a 2.5W ultra low power consumption, while it features 11 ESIstream SERDES that operate synchronously with the sampling clock to help achieving a deterministic data transfer.

EV10AS940 also features Digital Down Conversion (DDC) functionality with multiple options for decimation rates and up to 4 independent NCOs to support Fast Frequency Hopping in multiband operations. Coherent Frequency Hopping is possible thanks to multiple phase accumulators on each NCO and deterministic dedicated hopping trigger I/Os.

Digital integer and fractional delays enable Beam Forming capability allowing the EV10AS940 to be used in Phased Arrays applications.

Main features:

- 35.5GHz Bandwidth
- 2.5W power consumption
- On chip calibration
- 4 DDC channels, with decimation ratios from 2 to 1023
- Fast,Deterministic & Coherent Frequency Hopping
- ESIstream 62/64b SERDES protocol
- Multi-AS940 synchronization capability

4. SPECIFICATION

4.1 Electrical Characteristics for Supplies, Inputs and Outputs

Unless otherwise specified, typical values are given at Tj=85°C with Fs=12.8GSps, no DDC activated, no background calibration, NCO_CLK, SSO2 and SYNCO disabled, and for the following typical supplies V_{CCA3V3} = 3.3V, V_{CCA1V2} = 1.2V, V_{CCA0V9} = 0.9V, V_{CCD0V9} = 0.9V, V_{CCO0V9} = 0.9V, V_{CCO1V8} = 1.8V, V_{CCS1V8} = 1.8V
The considered junction temperature T_j is that of the hotspot. Minimum and Maximum values are given over temperature.

Table 1 : Electrical Characteristics for Supplies, Inputs and Outputs.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
RESOLUTION	5			10		bit
POWER REQUIREMENTS						
Power Supply voltage						
- Analog 3.3V		V_{CCA3V3}	3.2	3.3	3.4	V
- Analog 1.2V		V_{CCA1V2}	1.15	1.2	1.25	V
- Analog 0.9V		V_{CCA0V9}	0.85	0.9	0.95	V
- Digital		V_{CCD0V9}	0.85	0.9	0.95	V
- High Speed Serial-Links		V_{CCO0V9}	0.85	0.9	0.95	V
- GPIO		V_{CCO1V8}	1.70	1.8	1.90	V
- SPI		V_{CCS1V8}	1.15	1.2/1.5/1.8	1.90	V
Power Supply current						
- Analog 3.3V		I_{CCA3V3}		415	420	mA
- Analog 1.2V		I_{CCA1V2}		511	704	mA
- Analog 0.9V		I_{CCA0V9}		104	144	mA
- Digital		I_{CCD0V9}		212	252	mA
- HS Serial-links						
• full swing		I_{CCO0V9}		158	177	mA
• reduced swing		I_{CCO0V9}		120	128	mA
- GPIO		I_{CCO1V8}		5	7	mA
- SPI		I_{CCS1V8}		5	6	mA
Power dissipation Full analog power mode		P_D				
• Full swing				2.43	2.85	W
• Reduced swing				2.38	2.80	W
ANALOG INPUT (VIN)						
Common mode compatibility for analog inputs		AC				
Full-Scale input voltage range		V_{IN-pp}			500	mVpp
Analog input power level (in 50Ω termination)		P_{IN}			-2	dBm
Input leakage current		I_{IN}		TBD		µA
Input resistance (single)		R_{IN}	40	50	60	Ω
CLOCK INPUT (CKIN)						
Common mode compatibility for clock input		AC				
Intrinsic clock jitter (1)				28		fs_{rms}
Clock input power level in 50Ω		P_{CLK}		2		dBm
Clock single input voltage		$\lvert V_{CLK} \rvert$		800		mVpp
Clock input slew rate (square or sinewave clock)		SR_{CLK}			40	GV/s
Clock input capacitance (die + package)		C_{CLK}		TBD		pF
Clock input resistance (single)		R_{CLK}	40	50	60	Ω
Clock duty cycle		Duty Cycle	45	50	55	%
CMOS INPUTS SPI (CSN, RSTN, SCLK, MOSI), FREQUENCY HOPPING (NCO_SEL0, NCO_SEL1, NCO_SEL2)						
Low level threshold of Schmitt trigger		$V_{TminusC}$			0.30*V_{CCS1V8}	V
High level threshold of Schmitt trigger		V_{TplusC}	0.70*V_{CCS1V8}			V

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
CMOS Schmitt trigger hysteresis		V_{HYSTC}	0.10*V_{CCS1V8}			V
CMOS low level input current (Vinc=0 V)		I_{ILC}			0.3	µA
CMOS high level input current (Vinc= V_{CCS1V8} max)		I_{IHC}			15	µA
CMOS OUTPUTS SPI (MISO), FREQUENCY HOPPING (NCO_CLK)						
CMOS low level output voltage (lolc = 3 mA)		V_{OLC}			0.20*V_{CCS1V8}	V
CMOS high level output voltage (lohc = 3 mA)		V_{OHC}	0.8*V_{CCS1V8}			V
SYNC INPUT (SYNCIN/P)						
Logic compatibility			LVDS			
Input voltages to be applied • Swing • Common mode (DC Coupled)		 V_{IH}-V_{IL} V_{ICM}	 100 1.00	 350 1.25	 600 1.50	 mV V
Input capacitance		CSYNC		0.5		pF
Input resistance		RSYNC	80	100	120	Ω
SYNC OUTPUTS (SYNCON/P, SSON/P, SSO2N/P)						
Logic compatibility			LVDS			
Output levels (full swing) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination) • Logic low • Logic high • Differential output • Common mode (2)		 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}	 1.25 250 1.025	 350 1.25	 1.25 450 1.375	 V V mV V
Outputs levels in power down mode		Outp/Outn		1.8		V
High Speed Serial Links OUTPUTS (SLxN/P with x = 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 10)						
Logic compatibility			CML			
Operating mode			Synchronous			
Output levels (full swing) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination • Logic low • Logic high • Differential output • Common mode		 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}		 V_{CCO0V9}-0,55 V_{CCO0V9}-0.21 170 V_{CCO0V9}-0,38		 V V mVp V
Output levels (reduce swing) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination • Logic low • Logic high • Differential output • Common mode		 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}		 V_{CCO0V9}-0,41 V_{CCO0V9}-0.15 130 V_{CCO0V9}-0.28		 V V mVp V

(1) Intrinsic jitter integrated from 1Hz to 29GHz.
(2) DC coupled mandatory for SYNCON/P.

4.2 Converter's Characteristics

Unless otherwise specified, typical values are given at Tj=85°C with Fs=12.8GSps, P_{CLK} = +2dBm, no DDC activated, no background calibration, NCO_CLK, SSO2 and SYNCO disabled, and for the following typical supplies V_{CCA3V3} = 3.3V, V_{CCA1V2} = 1.2V, V_{CCA0V9} = 0.9V, V_{CCD0V9} = 0.9V, V_{CCO0V9} = 0.9V, V_{CCO1V8} = 1.8V, V_{CCS1V8} = 1.8V
Minimum and Maximum values are given over temperature.

Table 2 : Dynamic Characteristics.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC ANALOG INPUT						
Full power input bandwidth (-3dB)		FPBW		34		GHz
DYNAMIC PERFORMANCE						
Spurious Free Dynamic Range (Single Tone) Fin=6.7 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin=15.6 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 28,2 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 34.5 GHz • -6 dBFS		SFDR		 40 45 49 40 45 50 43 47 50 41		dBc
SNR Fin=6.7 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin=15.6 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 28.2 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 34.5 GHz • -1 dBFS • -3 dBFS • -6 dBFS		SNR		 45 46 46 42 43 45 40 42 45 39 41 44		dBFS
ENOB Fin=6.7GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin=15.6 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 28.2GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 34.5GHz • -1 dBFS • -3 dBFS • -6 dBFS		ENOB		 6.3 6.8 7.3 6.3 6.8 7.2 6.4 6.7 7.2 6.2 6.5 7.0		bits

5. PIN CONFIGURATION AND FUNCTIONS

5.1 Pinout Top View

Figure 2 : EV10AS940 Pinout.

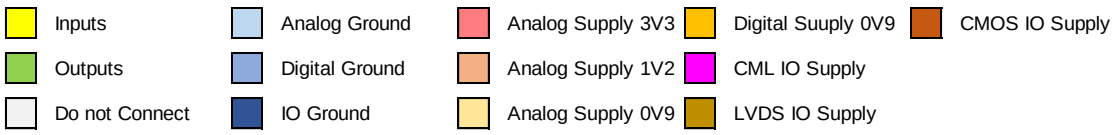

Figure 3 : Pinout Color Description.

6. PACKAGE DESCRIPTION

6.1 Package Substrate Description

EV10AS940 package consists of a Flip-Chip Ball Grid Array (FC-BGA) organic substrate and Copper lid with Nickel finishing. The details of the package are:

- Package Technology: FC-BGA
- Package Dimensions: 16.0x17.6mm²
- Ball Count: 350
- Ball Pitch: 0.8mm
- Ball Diameter: 0.5mm
- Ball Material: SAC305
- RoHS: Pb-Free

6.2 Package Outline

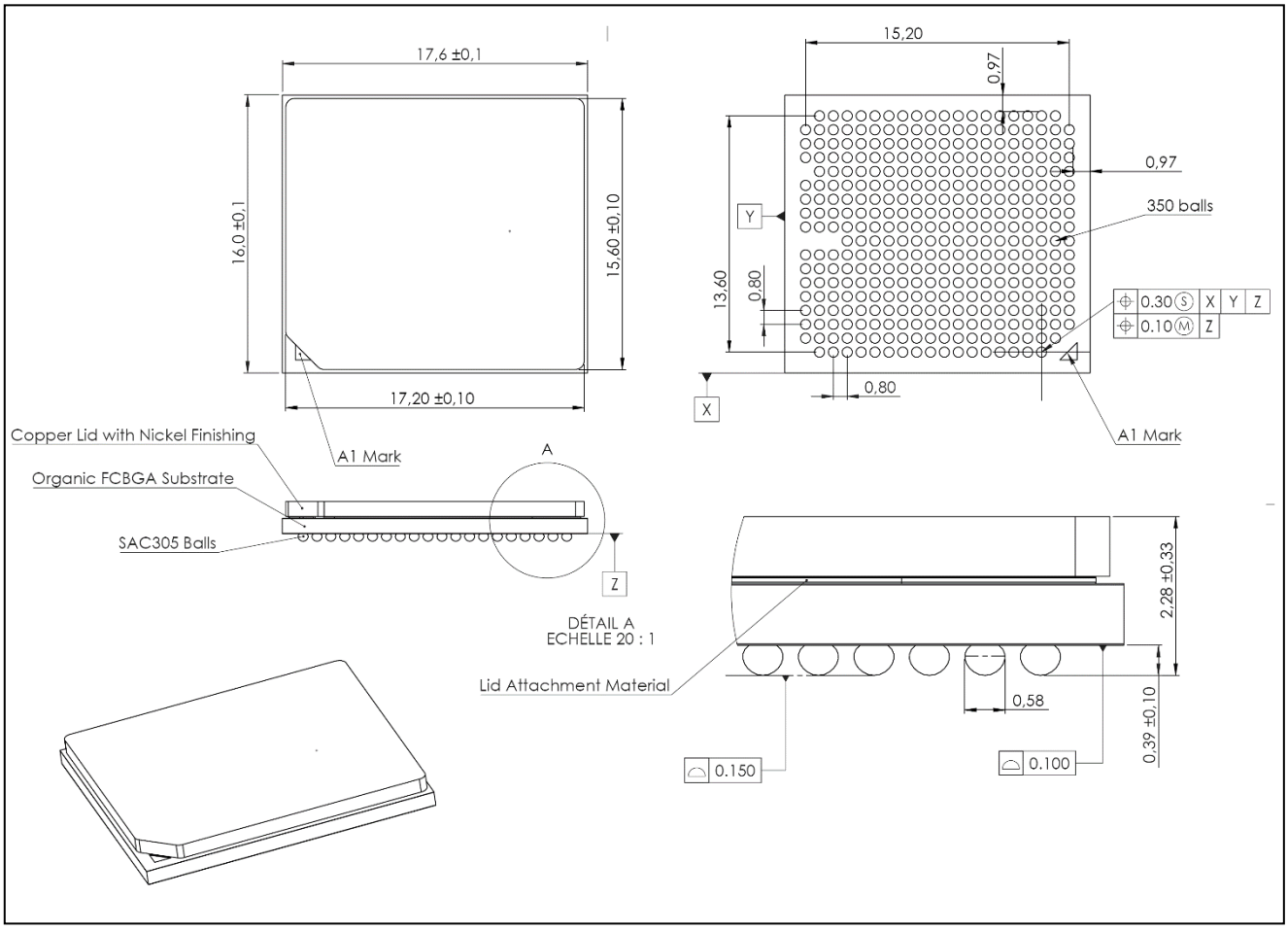

Figure 4 : EV10AS940 BGA Package Outline. (1)

(1) All dimensions in mm.

7. ORDERING INFORMATION

Table 3 : Product Ordering Information.

Part Number	Package	Temperature Range	Screening Level	RoHS	Comment
EVP10AS940ZJ	FC-BGA350	Ambient	Prototype	Pb-Free	Prototype

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